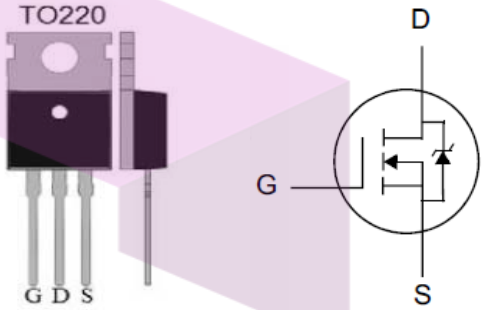
40V N-Channel MOSFET

Lead Free Package and Finish

BV_{DSS}	$R_{DS(ON),typ.}$	I_D[2]
40V	1.6mΩ	280A

General Features

- Proprietary New Trench Technology
- $R_{DS(ON),typ.}$=1.6 m Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode



Applications

- High efficiency DC/DC Converters
- Synchronous Rectification
- UPS Inverter

Ordering Information

Part Number	Package	Brand
PTP02N04N	TO-220	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	PTP02N04N	Unit
V_{DSS}	Drain-to-Source Voltage[1]	40	V
V_{GSS}	Gate-to-Source Voltage	±20	
I_D	Continuous Drain Current[2]	280	A
	Continuous Drain Current[3]	80	
	Continuous Drain Current @ Tc=100℃[2]	210	
I_{DM}	Pulsed Drain Current at V_{GS}=10V[2,4]	1080	
E_{AS}	Single Pulse Avalanche Energy	722	mJ
dv/dt	Peak Diode Recovery dv/dt[3]	5.0	V/ns
P_D	Power Dissipation	300	W
	Derating Factor above 25℃	2.0	W/℃
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 175	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTP02N04N	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	

Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	40	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	5	uA	V_{DS}=40V, V_{GS}=0V
		--	--	100		V_{DS}=32V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+20V, V_{DS}=0V
		--	--	-100		V_{GS}=-20V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	1.6	2.0	mΩ	V_{GS}=10V, I_D=80A [5]
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	12.8	--	nF	V_{GS}=0V, V_{DS}=25V, f=1.0MH_Z
C_{rss}	Reverse Transfer Capacitance	--	0.37	--		
C_{oss}	Output Capacitance	--	1.1	--		
R_G	Gate Series Resistance	--	3.6	--	Ω	f=1.0MH_Z
Q_g	Total Gate Charge	--	129	--	nC	V_{DD}=20V, I_D=100A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	33	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	24	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	27	--	nS	V_{DD}=20V, I_D=50A, V_{GS}= 10V R_G=10Ω
t_{rise}	Rise Time	--	85	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	203	--		
t_{fall}	Fall Time	--	96	--		

Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current[2]	--	--	280	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	1080		
V_{SD}	Diode Forward Voltage	--	0.90	1.2	V	I_S=80A, V_{GS}=0V
trr	Reverse recovery time	--	55	--	ns	V_{GS}=0V ,I_F=100A, di_F/dt=100A/μs
Qrr	Reverse recovery charge	--	43	--	nC	

Note:

[1] T_J=+25℃ to +175℃ .
[2] Silicon limited current only.
[3] Package limited current.
[4] Repetitive rating; pulse width limited by maximum junction temperature.
[5] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

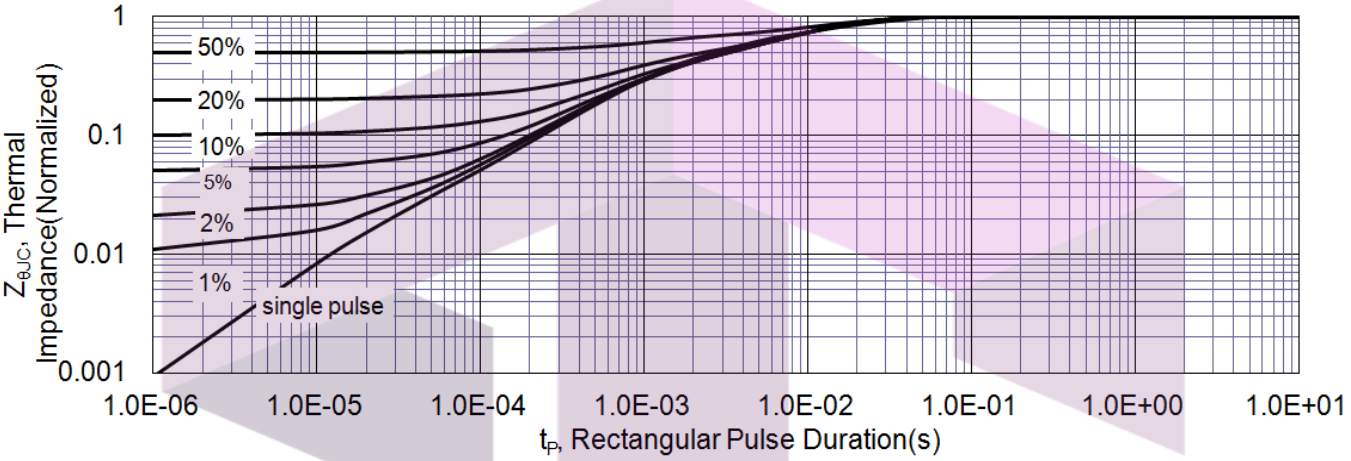


Figure 2. Maximum Power Dissipation vs Case Temperature

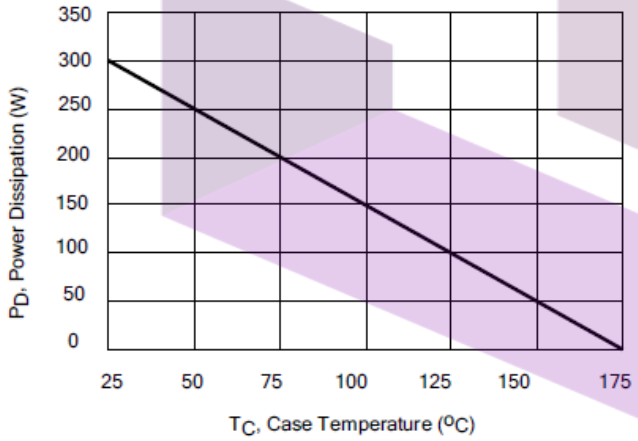


Figure3. Maximum Continuous Drain Current vs Case Temperature

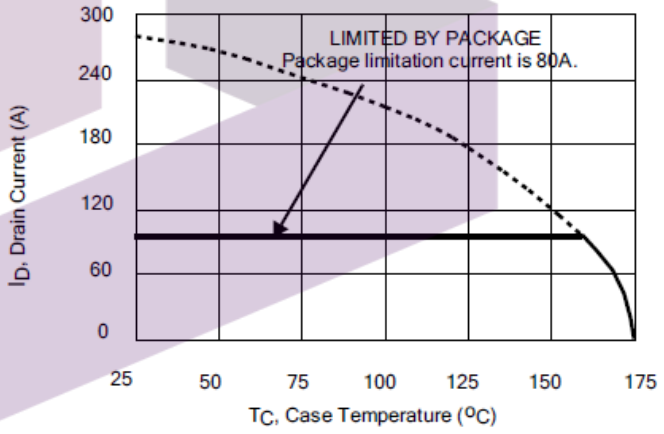


Figure 4. Typical Output Characteristics

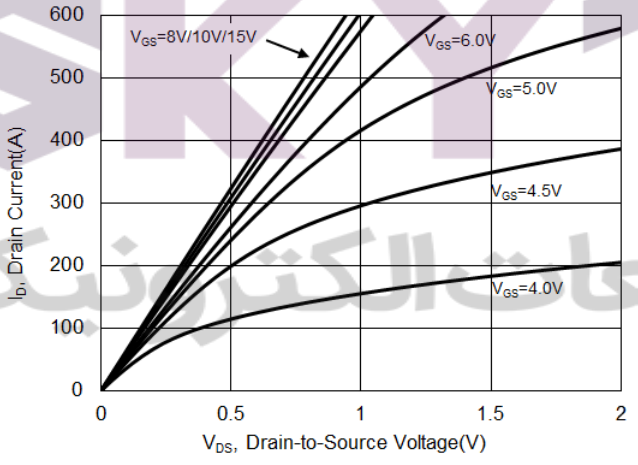
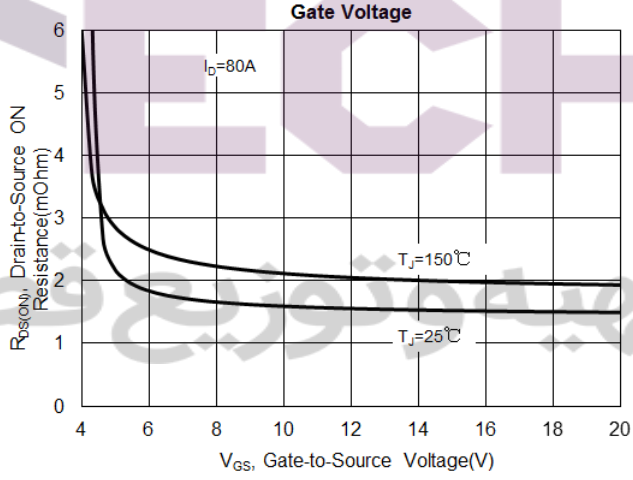


Figure 5. Typical Drain-to-Source ON Resistance vs. Gate Voltage



Typical Characteristics(Cont.)

Figure 6. Maximum Peak Current Capability

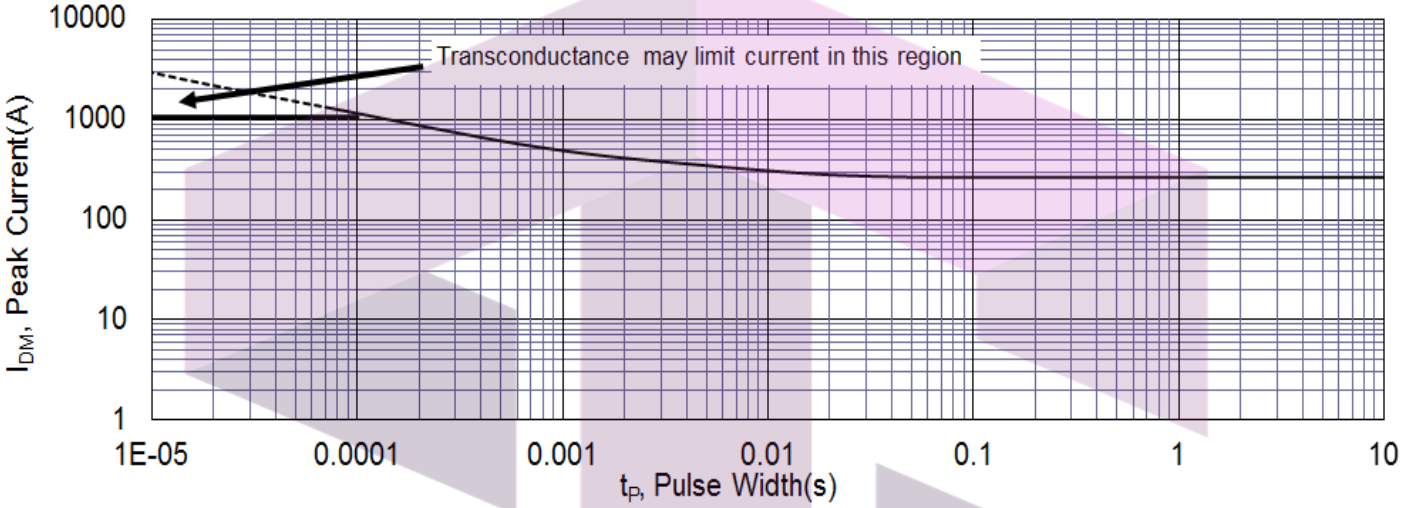


Figure 7. Typical Transfer Characteristics

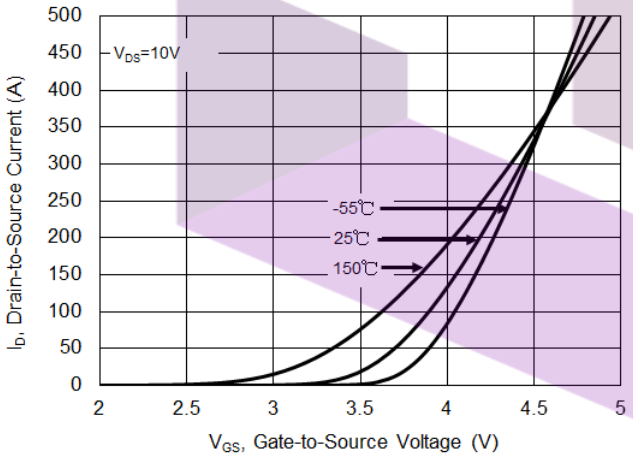


Figure 8. Unclamped Inductive Switching Capability

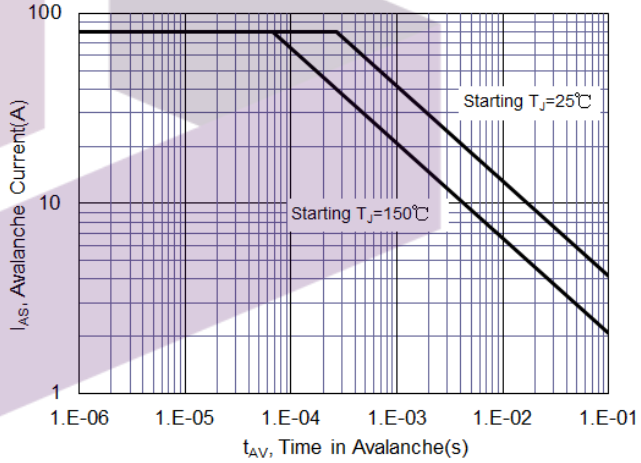


Figure 9. Typical Drain-to-Source ON Resistance

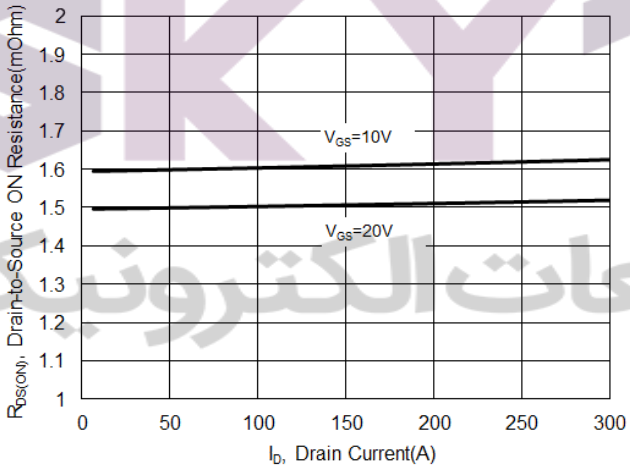
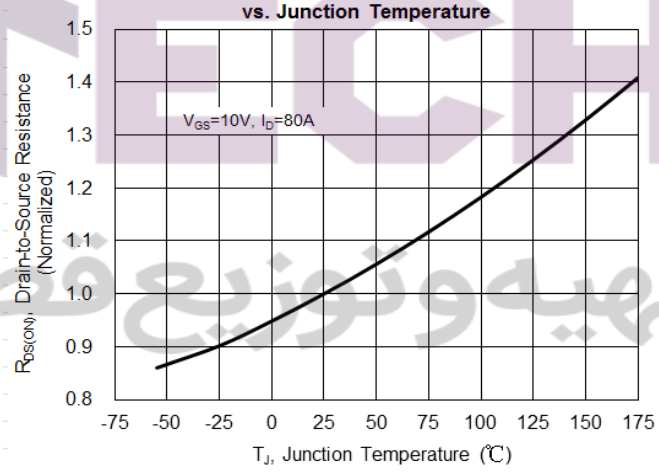


Figure 10. Typical Drain-to-Source On Resistance vs. Junction Temperature



Typical Characteristics(Cont.)

Figure 11.Typical Breakdown Voltage vs. Junction Temperature

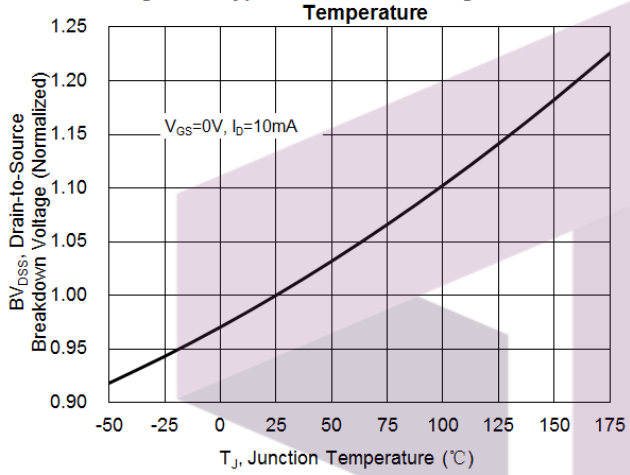


Figure 12.Typical Threshold Voltage vs. Junction Temperature

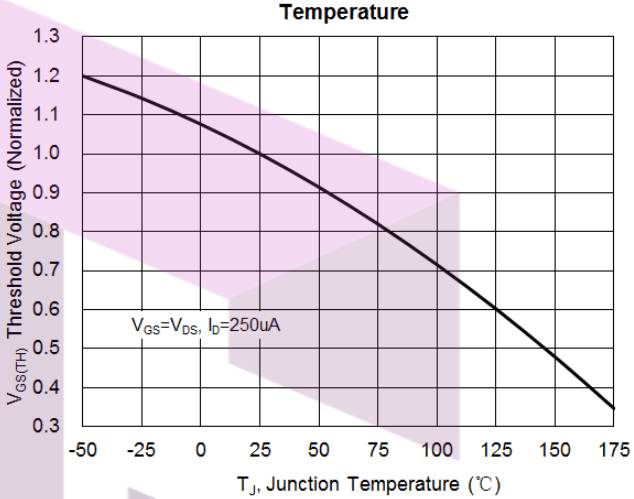


Figure 13. Maximum Forward Safe Operation Area

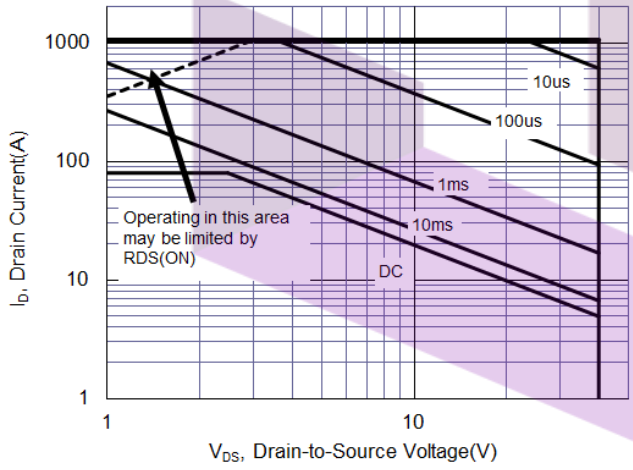


Figure 14. Typical Capacitance vs. Drain-to-Source Voltage

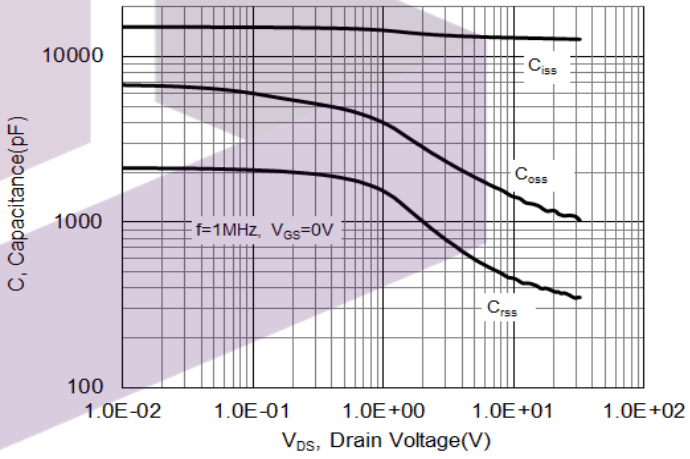


Figure 15. Typical Gate Charge vs. Gate-to-Source Voltage

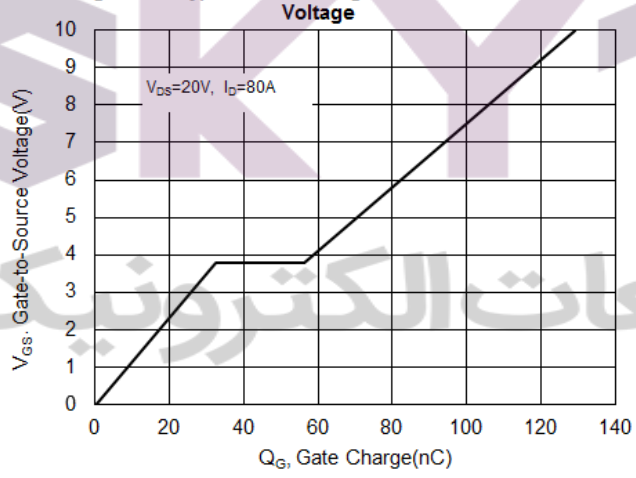
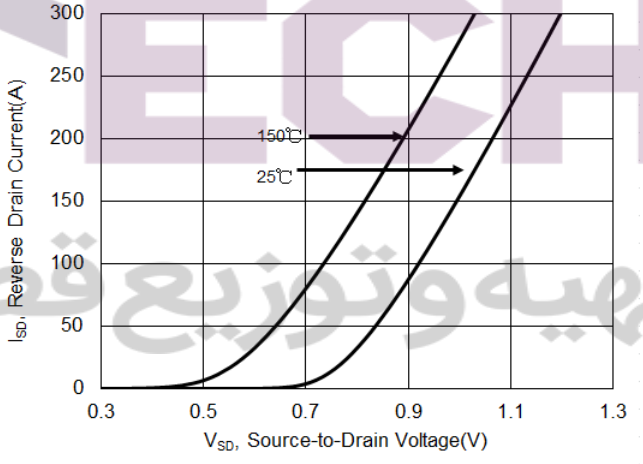


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

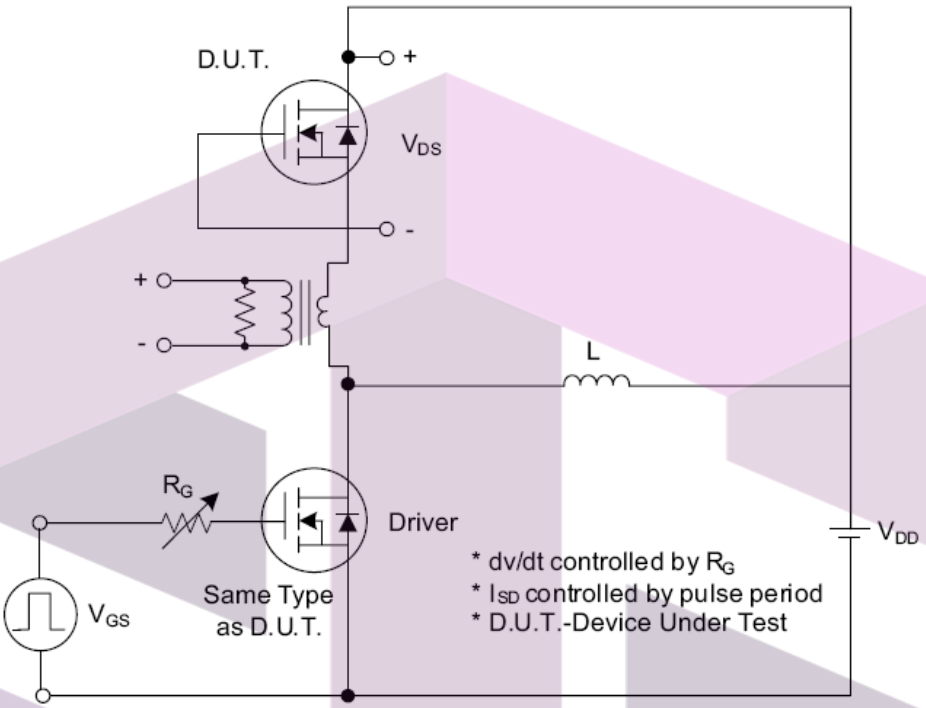


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

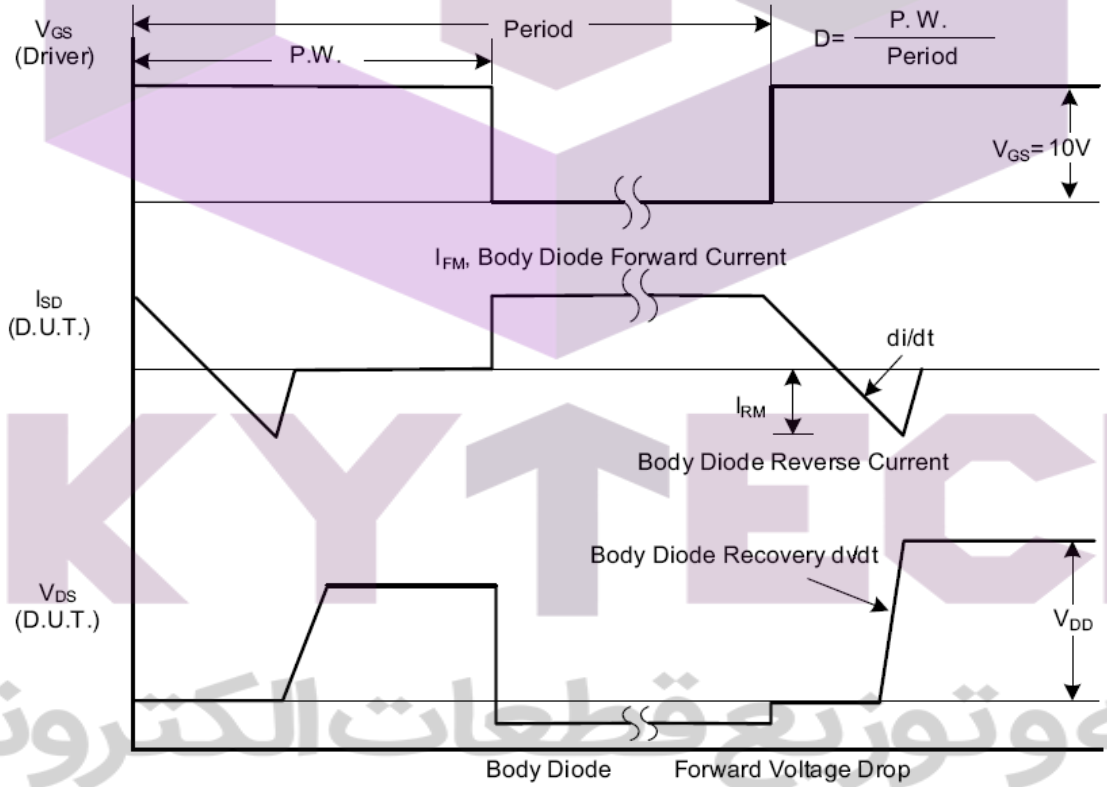


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

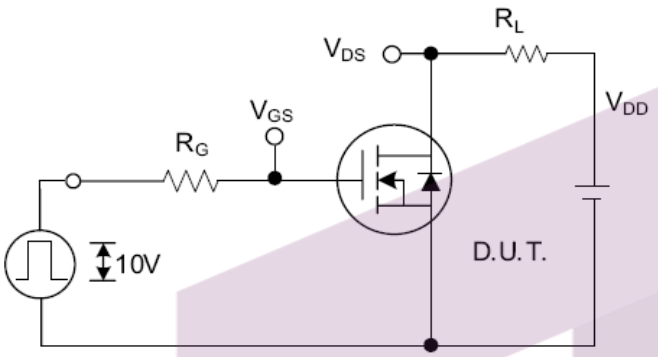


Fig. 2.1 Switching Test Circuit

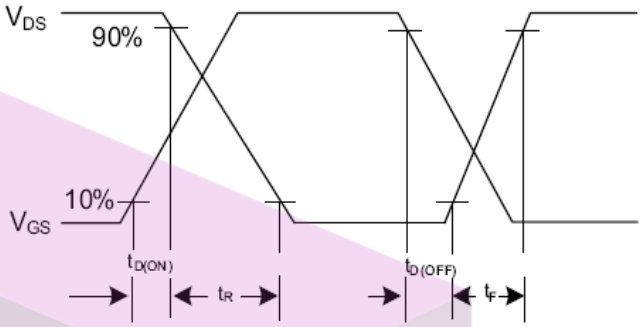


Fig. 2.2 Switching Waveforms

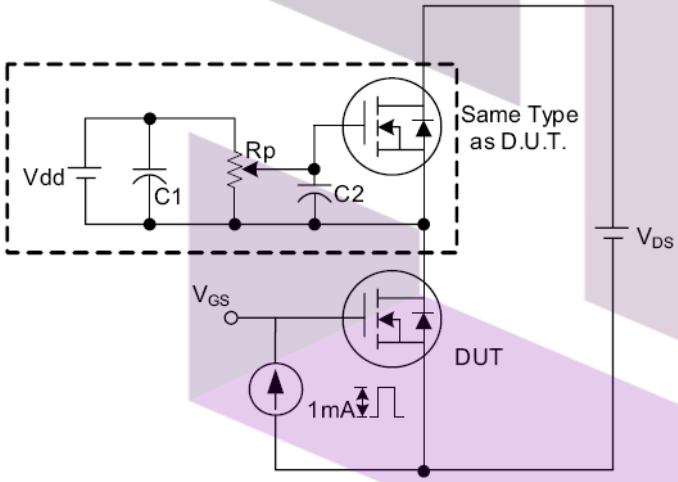


Fig. 3 . 1 Gate Charge Test Circuit

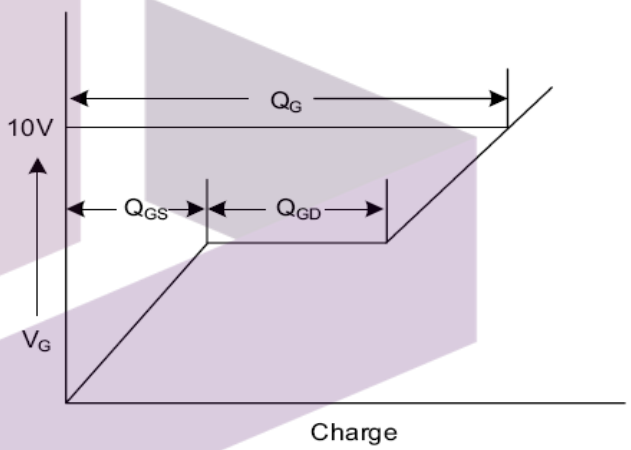


Fig. 3 . 2 Gate Charge Waveform

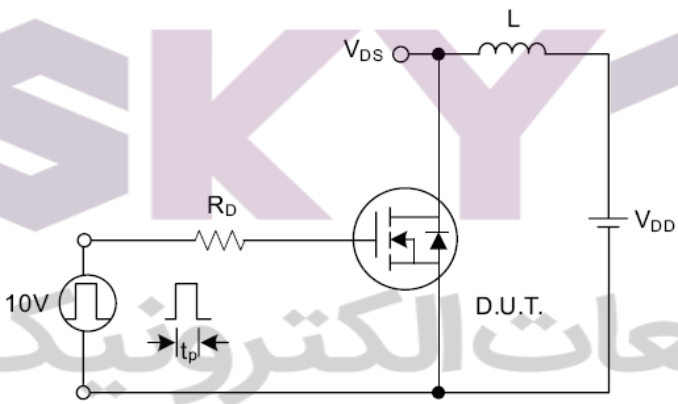


Fig. 4.1 Unclamped Inductive Switching Test Circuit

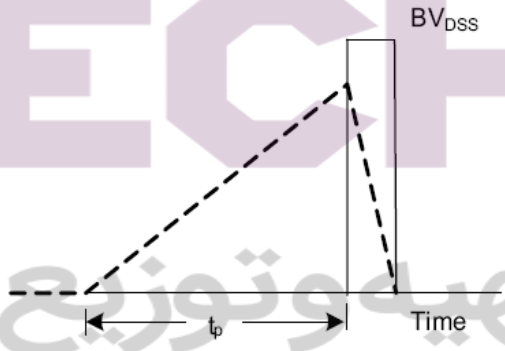


Fig. 4.2 Unclamped Inductive Switching Waveforms

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